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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/541,857

04/03/2000

James Digby Collier

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03/01/2005

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EXAMINER

LAM, TUAN THIEU

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental
Office Action Summary

Application No.

09/541,857

Applicant(s)

COLLIER ET AL.

Examiner

Tuan T. Lam

Art Unit

2816

CM

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 November 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 59-88 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 59-88 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

This is a response to the amendment filed 11/29/2004. Claims 59-88 are pending and are under examination. Applicant is advised to disregard the Office action dated on 1/27/2005.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 59-70, 72-73, 75-82 and 84-85 are rejected under 35 U.S.C. 102(b) as being anticipated by Kouno (JP 60-224319).

Figure 9 of Kouno shows a frequency divider circuit comprising a first signal means (not shown) for generating a first periodic signal (CL1) to be frequency divided by the frequency divider, said frequency divider comprises an input terminal for receiving the first periodic signal, an even number of amplifier stages (two amplifier stages 6-8; 9-11) connected in series, with an output of a last amplifier stage (9-11) connected to input of a first amplifier stage (6-8) and each amplifier each having an associated propagation delay and a transistor (7-8; 9-11) coupled between a supply terminal Vdd and a reference terminal (VSS) for modulating delay through the associated amplifier, the first periodic signal (CL1) applied to the first input terminal to a control electrode of the transistor of the odd amplifier stage (6-8), and for applying the second clock signal (CL2) to a control electrode of said transistor of the even amplifier (9-11) to modulate the propagation delays through the associated amplifier stages about half the period of said first and second periodic signals so that when the propagation delay through the even amplifier stage (9-

11) decreases, the propagation delay through the odd amplifier stage increases, and an output terminal (Q, Q/) for outputting a generated frequency divided signal, although, the first and second generating means are not shown, the transistors of the frequency divider are capable of receiving analog period signals so that not fully open and fully closed but to act as variable resistance as called for in claims 59, 75, 84 and 85.

1. Regarding claim 60, the number of amplifiers is two.
2. Regarding claim 61, Kouno shows a single frequency divider. However, it is known and obvious to one skilled in the art to cascade a plurality of Suzuki et al.'s frequency divider to obtain a desired frequency divided signal. Therefore, the limitation of cascading a plurality of frequency dividers will not be patentable under 35USC 103(a).
3. Regarding claims 62 and 76, each amplifier stage 6-8; 9-11 comprises differential amplifier.
4. Regarding claim 63, logic circuitry includes said transistor in each amplifier stage is seen as transistors in boxes 7, 8 and 10, 11.
5. Regarding claims 64, 77 and 79, each amplifier stage of Kouno inherently has hysteresis characteristics which varies in response to the clock signals.
6. Regarding claim 78, the limitations recited therein is inherently present in Kouno.
7. Regarding claims 65-67 and 80-81 each amplifier stage is CMOS.
8. Regarding claims 68 and 69, said first transistors are seen as transistors in boxes 7-8 for the odd stage 6-8, and for the even stage 242, said second transistors are seen as the transistors in boxes 10, 11. Said first and second transistors are coupled in series between the supply terminal and the reference terminal.

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9. Regarding claims 70 and 82, Kouno does not specifically indicate the periodic signal (CLOCK) in a range of 100 Mhz. However, it is known that CMOS technology is capable of operating with frequencies of 100 Mhz or higher. Therefore, the limitation of using the clock signal at 100 Mhz is seen to be inherently present in Kouno's frequency divider.

10. Regarding claim 72, first and second inverters are seen as transistors 6 and 9.

11. Regarding claim 73, N channel transistors are seen as transistors in boxes 7, 8, 10, 11.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 74 is rejected under 35USC 103(a) as being unpatentable over Kouno (JP 60-224319). The Kouno reference discloses all the aspects of the present invention as noted above except Kouno does not disclose the size of n channel controlling transistors (7, 8) is larger than the size of n channel transistors (the n channel transistors of the inverters in boxes 6). However, it is notoriously well known to implement the n channel controlling transistors with a larger size in order to reset the crossed inverters (6; 9) at a quicker speed thus preventing an erroneous operation. Therefore, the limitation of having n channel controlling transistor at a larger size than the size of the n channel inverting transistors will not be patentable under 35USC 103(a).

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12. Claims 71 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouno (JP 60-224319) in view of Maemura (USP 5,172,400). The Kouno reference discloses all the aspects of the present invention as noted above except logic circuitry connected in series between at least two of the amplifier stages in order to enable division by ratios other than simple powers of two as called for in claims 71 and 83. Figure 15 of Maemura reference teaches the use of a logic circuitry (41) implemented in between two amplifier stage to obtain a division ratio other than power of two. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to include the logic circuitry (41) of Maemura in the circuit arrangement of Kouno's figure 9 for the flexibility of obtaining a frequency divided output other than power of two.

13. Claims 87 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouno (JP 60-224319). The Kouno reference discloses all the aspects of the present invention as noted above except Kouno does not disclose first and second generating means formed by a single circuit as called for in claims 87 and 88. Although, the first and second generating means are not shown inn Konno, the transistors of the frequency divider are capable of receiving analog period signals so that not fully open and fully closed but to act as variable resistance. It is obvious to one skilled in art to form the first and second generating circuits in one single circuit in order to save space on an integrated chip and to reduce manufacturing cost. Therefore, outside of an non-obvious results the obviousness of forming the first and second generating circuit on a single circuit to save space on an integrated chip and to reduce manufacturing cost will not be patentable under 35USC 103(a).


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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Tuan T. Lam
Primary Examiner
Art Unit 2816

2/22/2005